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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/886,368	Applicant(s) HAMAMOTO ET AL.	
	Examiner Kandasamy Thangavelu	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *46-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *46-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' Amendment mailed on May 6, 2003, 2003. Claims 46-60 of the application are pending.

Response to Amendments

2. Applicants' amendments, filed on May 6, 2003 have been considered. The applicants have indicated claims 46-54 as cancelled. However, the applicants have not requested the office to cancel the claims 46-54. So the examiner has treated the claims 46-54 as pending in the application. The rejections based on the newly cited reference(s) follow. Therefore, this office action is made non-final.

The applicants have referred to Examiner notice in previous Office Action. The examiner requests the applicants' attention to the fact that the previous Office Action did not include any Examiner's notice.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

4. The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 46, 47 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kramer et al. (KKR)** (U.S. Patent 4,667,0880) in view of **Mita et al. (MI)** (U.S. Patent 5,081,672).

5.1 **KKR** teaches a portable data processing and storage system. Specifically, as per Claim 46, **KKR** teaches a memory apparatus having a playback function removably connected with a digital signal source to store digital data received from the digital signal source (Col 1, Line 61 to Col 2, Line 24; Col 4, Lines 6-8; Col 6, Lines 24-28);

to reproduce the digital data stored therein independently of the digital signal source (Col 1, Line 61 to Col 2, Line 24); and

the memory apparatus comprising a built-in playback circuit, including a digital-to-analog converter, a filter circuit and an audio amplifier, for reproducing digital data stored in the memory circuit (Col 1, Line 61 to Col 2, Line 24; Col 1, Lines 56-60; Col 5, Lines 39-44; Col 5, Lines 58-64; Col 6, Lines 6-12).

KKR does not expressly teach that the memory apparatus has a built-in memory circuit formed of a semiconductor memory for storing digital data received with addresses of the digital

data from the digital signal source. **MI** teaches that the memory apparatus has a built-in memory circuit formed of a semiconductor memory for storing digital data received with addresses of the digital data from the digital signal source (Col 1, Lines 25-33; Col 3, Lines 1-12), as high speed recording and reproduction of audio data can be achieved with memory circuit having semiconductor memory (Col 1, Lines 67-68; Col 3, Lines 1-9). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the memory apparatus of **KKR** with the memory apparatus of **MI** that included a built-in memory circuit formed of a semiconductor memory for storing digital data received with addresses of the digital data from the digital signal source, as high speed recording and reproduction of audio data could be achieved with memory circuit having semiconductor memory.

5.2 As per Claim 47, **KKR** and **MI** teach the memory apparatus of claim 46. **KKR** also teaches that the digital data is transmitted by communication means (Col 2, Lines 48-50).

5.3 As per Claim 49, **KKR** and **MI** teach the memory apparatus of claim 46. **KKR** teaches that the memory apparatus is a card-like storage medium (Col 1, Line 61 to Col 2, Line 24; Col 4, Lines 6-8; Col 6, Lines 24-28).

6. Claim 48 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Kramer et al. (KKR)** (U.S. Patent 4,667,0880) in view of **Mita et al. (MI)** (U.S. Patent 5,081,672), and further in view of **Jinguji (JI)** (U.S. Patent 4,847,840).

6.1 As per Claim 48, **KKR** and **MI** teach the memory apparatus of claim 46. **KKR** and **MI** do not expressly teach that the built-in playback circuit has playback conditions which are automatically designated in accordance with the contents of an identification (ID) code. **JI** teaches that the built-in playback circuit has playback conditions which are automatically designated in accordance with the contents of an identification (ID) code (Col 12, Lines 63-67; Col 12, Lines 47-49), as the identification data indicate if the audio data is monaural or stereo data and the sampling frequency to be used (Col 12, Lines 63 to Col 13, Line 16). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the built-in playback circuit of **KKR** and **MI** with identification (ID) code of **JI** that included playback conditions which are automatically designated, as the identification data would indicate if the audio data was monaural or stereo data and the sampling frequency to be used.

7. Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Kramer et al. (KKR)** (U.S. Patent 4,667,0880) in view of **Mita et al. (MI)** (U.S. Patent 5,081,672), and **Jinguji (JI)** (U.S. Patent 4,847,840), and further in view of **Hyatt (HY)** (U.S. Patent 5,339,275), and **Kasuga (KA)** (U.S. Patent 4,542,369).

7.1 As per Claim 50, **KKR** and **MI** teach the memory apparatus of claim 46. **KKR** and **MI** do not expressly teach that the playback circuit has playback conditions which include stereo or monaural playback. **JI** teaches that the playback circuit has playback conditions which include stereo or monaural playback (Col 12, Lines 43-45; Col 12 Line 67 to Col 13 Line 5), as the sampling frequency used depends on if the audio data is monaural or stereo data (Col 13, Lines

6-8). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the built-in playback circuit of **KKR** and **MI** with the playback circuit of **JI** that included playback conditions which included stereo or monaural playback, as the sampling frequency used would depend on if the audio data is monaural or stereo data.

KKR does not expressly teach that the playback circuit has playback conditions which include a sampling frequency. **JI** teaches that the playback circuit has playback conditions which include a sampling frequency (Col 13, Lines 6-16). As per **MI**, the memory required to store the data could be minimized by decreasing the sampling frequency (Col 2, Lines 4-6) and the sampling frequency affects the quality of the audio which is stored and reproduced (Col 2, Lines 50-53). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the built-in playback circuit of **KKR** with the playback circuit of **JI** that included playback conditions which included a sampling frequency, as as per **MI**, the memory required to store the data could be minimized by decreasing the sampling frequency and the sampling frequency would affect the quality of the audio which would be stored and reproduced.

KKR, MI and **JI** do not expressly teach that the playback circuit has playback conditions which include a resolution of 8 and 16 bits. **HY** teaches that the playback circuit has playback conditions which include a resolution of 8 bits (Col 56, Lines 24-39), as an improvement in storage capacity could be achieved when 8-bit resolution audio information is stored Col 56, Lines 34-35). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the built-in playback circuit of **KKR, MI** and **JI** with playback

conditions of **HY** which included a resolution of 8 bits, as an improvement in storage capacity could be achieved when 8-bit resolution audio information is stored.

KKR, MI and **JI** do not expressly teach that the playback circuit has playback conditions which include a resolution of 16 bits. **KA** teaches that the playback circuit has playback conditions which include a resolution of 16 bits (Col 3, Lines 57-61), as signal transmission of particularly high quality could be achieved with 16 bits resolution (Col 3, Lines 57-61). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the built-in playback circuit of **KKR, MI** and **JI** with playback conditions of **KA** which included a resolution of 16 bits, as signal transmission of particularly high quality could be achieved with 16 bits resolution.

8. Claims 51 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kramer et al. (KKR)** (U.S. Patent 4,667,0880) in view of **Mita et al. (MI)** (U.S. Patent 5,081,672), and further in view of **Samph et al. (SA)** (U.S. Patent 5,204,813) and **Koenck (KO)** (U.S. Patent 4,737,702).

8.1 As per Claim 51, **KKR** teaches a memory apparatus having a playback function removably connected with a digital signal source to store digital data received from the digital signal source (Col 1, Line 61 to Col 2, Line 24; Col 4, Lines 6-8; Col 6, Lines 24-28);

to reproduce the digital data stored therein independently of the digital signal source (Col 1, Line 61 to Col 2, Line 24); and

the memory apparatus comprising a built-in playback circuit, including a digital-to-analog converter, a filter circuit and an audio amplifier, for reproducing digital data stored in the memory circuit (Col 1, Line 61 to Col 2, Line 24; Col 1, Lines 56-60; Col 5, Lines 39-44; Col 5, Lines 58-64; Col 6, Lines 6-12).

KKR does not expressly teach that the memory apparatus has a built-in memory circuit formed of a semiconductor memory for storing digital data received with addresses of the digital data from the digital signal source. **MI** teaches that the memory apparatus has a built-in memory circuit formed of a semiconductor memory for storing digital data received with addresses of the digital data from the digital signal source (Col 1, Lines 25-33; Col 3, Lines 1-12), as high speed recording and reproduction of audio data can be achieved with memory circuit having semiconductor memory (Col 1, Lines 67-68; Col 3, Lines 1-9). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the memory apparatus of **KKR** with the memory apparatus of **MI** that included a built-in memory circuit formed of a semiconductor memory for storing digital data received with addresses of the digital data from the digital signal source, as high speed recording and reproduction of audio data could be achieved with memory circuit having semiconductor memory.

KKR and **MI** do not expressly teach that the memory apparatus has a rechargeable battery capable of being charged by a power supply in the digital signal source when the memory card is connected with the digital signal source. **SA** teaches that the memory apparatus has a rechargeable battery capable of being charged by a power supply in the digital signal source when the memory card is connected with the digital signal source (Fig. 3, Items 108, 120 and 122; Col 6, Lines 20-22; Col 7, Lines 30-40; Col 7, Lines 35-40), as the rechargeable battery

allows portable use of the memory apparatus (Col 6, Lines 20-22); and as per **KO**, the rechargeable battery provides increased useful life and reliability (Col 1, Lines 52-53). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the memory apparatus of **KKR** and **MI** with rechargeable battery capable of being charged by a power supply in the digital signal source when the memory card was connected with the digital signal source of **SA**, as the rechargeable battery would allow portable use of the memory apparatus; and as per **KO**, the rechargeable battery would provide increased useful life and reliability.

8.2 As per Claim 53, **KKR, MI, SA** and **KO** teach the memory apparatus of claim 51. **KKR** teaches that the memory apparatus is a card-like storage medium (Col 1, Line 61 to Col 2, Line 24; Col 4, Lines 6-8; Col 6, Lines 24-28).

9. Claim 52 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Kramer et al. (KKR)** (U.S. Patent 4,667,0880) in view of **Mita et al. (MI)** (U.S. Patent 5,081,672), **Samph et al. (SA)** (U.S. Patent 5,204,813) and **Koenck (KO)** (U.S. Patent 4,737,702), and further in view of **Jinguji (JI)** (U.S. Patent 4,847,840).

9.1 As per Claim 52, **KKR, MI, SA** and **KO** teach the memory apparatus of claim 51. **KKR, MI, SA** and **KO** do not expressly teach that the built-in playback circuit has playback conditions which are automatically designated in accordance with the contents of an identification (ID) code. **JI** teaches that the built-in playback circuit has playback conditions

which are automatically designated in accordance with the contents of an identification (ID) code (Col 12, Lines 63-67; Col 12, Lines 47-49), as the identification data indicate if the audio data is monaural or stereo data and the sampling frequency to be used (Col 12, Lines 63 to Col 13, 16). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the built-in playback circuit of **KKR, MI, SA** and **KO** with identification (ID) code of **JI** that included playback conditions which are automatically designated, as the identification data would indicate if the audio data was monaural or stereo data and the sampling frequency to be used.

10. Claim 54 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Kramer et al. (KKR)** (U.S. Patent 4,667,0880) in view of **Mita et al. (MI)** (U.S. Patent 5,081,672), **Samph et al. (SA)** (U.S. Patent 5,204,813), **Koenck (KO)** (U.S. Patent 4,737,702) and **Jinguji (JI)** (U.S. Patent 4,847,840), and further in view of **Hyatt (HY)** (U.S. Patent 5,339,275), and **Kasuga (KA)** (U.S. Patent 4,542,369).

10.1 As per Claim 54, **KKR, MI, SA** and **KO** teach the memory apparatus of claim 51. **KKR, MI, SA** and **KO** do not expressly teach that the playback circuit has playback conditions which include stereo or monaural playback. **JI** teaches that the playback circuit has playback conditions which include stereo or monaural playback (Col 12, Lines 43-45; Col 12 Line 67 to Col 13 Line 5), as the sampling frequency used depends on if the audio data is monaural or stereo data (Col 13, Lines 6-8). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the built-in playback circuit of **KKR, MI, SA** and

KO with the playback circuit of **JI** that included playback conditions which included stereo or monaural playback, as the sampling frequency used would depend on if the audio data is monaural or stereo data.

KKR, SA and **KO** do not expressly teach that the playback circuit has playback conditions which include a sampling frequency. **JI** teaches that the playback circuit has playback conditions which include a sampling frequency (Col 13, Lines 6-16). As per **MI**, the memory required to store the data could be minimized by decreasing the sampling frequency (Col 2, Lines 4-6) and the sampling frequency affects the quality of the audio which is stored and reproduced (Col 2, Lines 50-53). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the built-in playback circuit of **KKR, SA** and **KO** with the playback circuit of **JI** that included playback conditions which included a sampling frequency, as as per **MI**, the memory required to store the data could be minimized by decreasing the sampling frequency and the sampling frequency would affect the quality of the audio which would be stored and reproduced.

KKR, MI, SA, KO and **JI** do not expressly teach that the playback circuit has playback conditions which include a resolution of 8 and 16 bits. **HY** teaches that the playback circuit has playback conditions which include a resolution of 8 bits (Col 56, Lines 24-39), as an improvement in storage capacity could be achieved when 8-bit resolution audio information is stored Col 56, Lines 34-35). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the built-in playback circuit of **KKR, MI, SA, KO** and **JI** with playback conditions of **HY** which included a resolution of 8 bits, as an improvement in storage capacity could be achieved when 8-bit resolution audio information is stored.

KKR, MI, SA, KO and **JI** do not expressly teach that the playback circuit has playback conditions which include a resolution of 16 bits. **KA** teaches that the playback circuit has playback conditions which include a resolution of 16 bits (Col 3, Lines 57-61), as signal transmission of particularly high quality could be achieved with 16 bits resolution (Col 3, Lines 57-61). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the built-in playback circuit of **KKR, MI, SA, KO** and **JI** with playback conditions of **KA** which included a resolution of 16 bits, as signal transmission of particularly high quality could be achieved with 16 bits resolution.

11. Claims 55 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Kramer et al. (KKR)** (U.S. Patent 4,667,0880) in view of **Samph et al. (SA)** (U.S. Patent 5,204,813).

11.1 As per Claim 55, **KKR** teaches a memory apparatus having a playback function removably connected with a digital signal source to store digital data received from the digital signal source (Col 1, Line 61 to Col 2, Line 24; Col 4, Lines 6-8; Col 6, Lines 24-28); and

to reproduce the digital data stored therein independently of the digital signal source (Col 1, Line 61 to Col 2, Line 24); comprising:

a memory circuit for storing said digital data from the digital signal source (Col 1, Line 61 to Col 2, Line 24); and

a playback circuit for reproducing said digital data stored in said memory circuit (Col 1, Line 61 to Col 2, Line 24).

KKR does not expressly teach that the memory apparatus has an inner battery. **SA** teaches that the memory apparatus has an inner battery (Fig. 3, Items 108; Col 6, Lines 20-22), as the battery allows portable use of the memory apparatus (Col 6, Lines 20-22). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the memory apparatus of **KKR** with inner battery of **SA**, as the battery would allow portable use of the memory apparatus.

KKR does not expressly teach a battery switch, wherein the battery switch enables to use power from the digital source having a higher operating voltage than that of the inner battery when the memory circuit stores the digital data in a condition of connecting to the digital source. **SA** teaches a battery switch, wherein the battery switch enables to use power from the digital source having a higher operating voltage than that of the inner battery when the memory circuit stores the digital data in a condition of connecting to the digital source (Fig. 3, Items 102, 108, 120 and 122; Col 5, Lines 7-16; Fig. 4G; Col 10, Lines 14-39), as the memory card permits information to be transferred between the memory card and the digital source (personal computer) (Col 5, Lines 13-21); the battery switch allows to operably connect and disconnect the battery from the power supply circuit (Col 10, Lines 20-22) and the board is provided with a battery charging connector to electrically connect with mating terminals on the power supply to permit recharging the battery (Col 7, Lines 33-40). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the memory apparatus of **KKR** with the memory apparatus of **SA** that included a battery switch, wherein the battery switch enabled to use power from the digital source having a higher operating voltage than that of the inner battery when the memory circuit stored the digital data in a condition of connecting

to the digital source, as the memory card would permit information to be transferred between the memory card and the digital source; the battery switch would allow to operably connect and disconnect the battery from the power supply circuit and the board was provided with a battery charging connector to electrically connect with mating terminals on the power supply to permit recharging the battery.

KKR does not expressly teach a battery switch to use power from the inner battery when the playback circuit reproduces the digital data in a condition of being removed from the digital source. **SA** teaches a battery switch to use power from the inner battery when the playback circuit reproduces the digital data in a condition of being removed from the digital source (Fig. 3, Items 108; Col 6, Lines 20-25; Col 9, Lines 8-14; Col 10, Lines 14-39), as the inner battery allows portable use of the memory apparatus (Col 6, Lines 20-22). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the memory apparatus of **KKR** with the memory apparatus of **SA** that included a battery switch to use power from the inner battery when the playback circuit reproduced the digital data in a condition of being removed from the digital source, as the battery would allow portable use of the memory apparatus.

11.2 As per Claim 60, **KKR** and **SA** teach the memory apparatus of claim 55. **KKR** also teaches that the memory apparatus is a personal audio player for playing vended audio programs, and wherein the digital source is an audio program vending machine (Col 1, Line 64 to Col 2, Line 24; Col 6, Lines 24-30 and Lines 44-49).

12. Claim 56 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Kramer et al. (KKR)** (U.S. Patent 4,667,0880) in view of **Samph et al. (SA)** (U.S. Patent 5,204,813), and further in view of **Jinguji (JI)** (U.S. Patent 4,847,840).

12.1 As per Claim 56, **KKR** and **SA** teach the memory apparatus of claim 55. **KKR** and **SA** do not expressly teach that the digital data includes audio data and an identification (ID) code specifying a reproducing condition of the audio data, and the playback circuit reproduces the audio data following the reproducing condition. **JI** teaches that the digital data includes audio data and an identification (ID) code specifying a reproducing condition of the audio data, and the playback circuit reproduces the audio data following the reproducing condition (Col 12, Lines 63-67; Col 12, Lines 47-49), as the identification data indicate if the audio data is monaural or stereo data and the sampling frequency to be used (Col 12, Lines 63 to Col 13, Line 16). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the memory apparatus of **KKR** and **SA** with the memory apparatus of **JI** that included the digital data including audio data and an identification (ID) code specifying a reproducing condition of the audio data, and the playback circuit reproduced the audio data following the reproducing condition, as the identification data would indicate if the audio data was monaural or stereo data and the sampling frequency to be used.

13. Claim 57 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Kramer et al. (KKR)** (U.S. Patent 4,667,0880) in view of **Samph et al. (SA)** (U.S. Patent 5,204,813), and further in view of **Koguchi et al. (KOG)** (U.S. Patent 5,138,925).

13.1 As per Claim 57, **KKR** and **SA** teach the memory apparatus of claim 55. **KKR** and **SA** do not expressly teach that the ID code is inserted in the head of the digital data and is followed by the audio data, and the ID code and the audio data are integrally stored in the memory circuit. **KOG** teaches that the ID code is inserted in the head of the digital data and is followed by the audio data, and the ID code and the audio data are integrally stored in the memory circuit (Col 7, Lines 24-28; Col 7, Lines 41-47; Col 11, Lines 25-26; Col 12, Lines 28-29; Col 21, Lines 11-12), as the ID code indicates the type of message (Col 11, Lines 25-26). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the memory apparatus of **KKR** and **SA** with the memory apparatus of **KOG** that included the digital data including audio data and an identification (ID) code specifying a reproducing condition of the audio data, and the playback circuit reproduced the audio data following the reproducing condition, as the ID code would indicate the type of message.

14. Claim 58 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Kramer et al. (KKR)** (U.S. Patent 4,667,0880) in view of **Samph et al. (SA)** (U.S. Patent 5,204,813), and further in view of **Etoh et al. (ET)** (U.S. Patent 5,297,097).

14.1 As per Claim 58, **KKR** and **SA** teach the memory apparatus of claim 55. **KKR** and **SA** do not expressly teach a data transfer circuit to operate at an increased data transfer speed at the higher operating voltage from the digital source, in comparison to a data transfer speed at an operating voltage of the inner battery. **ET** teaches a data transfer circuit to operate at an

increased data transfer speed at the higher operating voltage from the digital source, in comparison to a data transfer speed at an operating voltage of the inner battery (Fig. 1C; Col 2, Lines 47-57; Col 5, Lines 7- 17; Col 8, Lines 6-29), as the performance of the system is greatly improved with higher voltage (Fig. 1C;Col 8, Lines 24-29). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the memory apparatus of **KKR** and **SA** with the memory apparatus of **ET** that included a data transfer circuit to operate at an increased data transfer speed at the higher operating voltage from the digital source, in comparison to a data transfer speed at an operating voltage of the inner battery, as the performance of the system would be greatly improved with higher voltage.

15. Claim 59 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Kramer et al. (KKR)** (U.S. Patent 4,667,0880) in view of **Samph et al. (SA)** (U.S. Patent 5,204,813), and further in view of **Koenck (KO)** (U.S. Patent 4,737,702).

15.1 As per Claim 59, **KKR** and **SA** teach the memory apparatus of claim 55. **KKR** does not expressly teach that the inner battery is a rechargeable battery. **SA** teaches that the inner battery is a rechargeable battery (Fig. 3, Items 108, 120 and 122; Col 6, Lines 20-22), as the rechargeable battery allows portable use of the memory apparatus (Col 6, Lines 20-22); and as per **KO**, the rechargeable battery provides increased useful life and reliability (Col 1, Lines 52-53). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the memory apparatus of **KKR** with the memory apparatus of **SA** that included a rechargeable battery, as the rechargeable battery would allow portable use of the

memory apparatus and as per **KO**, the rechargeable battery would provide increased useful life and reliability.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to the Applicants' disclosure.

The following patents are cited to further show the state of the art at the time of Applicants' invention with respect to memory apparatus with memory circuit of semiconductor memory, 8 bit and 16 bit resolution and rechargeable battery on portable memory cards.

1. Koguchi et al., "Apparatus for playing auto-play data in synchronism with audio data stored in a compact disc", U.S. Patent 5,138,925, August 1992.
2. Etoh et al., "Large scale integrated circuit for low voltage operation", U.S. Patent 5,297,097, March 1994.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 703-305-0043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-746-7329.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

K. Thangavelu
Art Unit 2123
June 4, 2003